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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,538	11/10/2003	Leroy Jones	016295.1455 (DC-05249)	5132

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,538	JONES, LEROY	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-21** are presented for examination.

Information Disclosure Statement

2. The references listed in the information disclosure statement submitted on 11/10/03 have been considered by the examiner (see attached PTO-1449).

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim objections

4. Claims **4, 6, 8, 9, 12, 13, 14, 16, 17, 20 and 21** are objected to because of the following informalities:

a) Please change the word "operable" to ---configured to operate--- (see claims 4, 6, 8, 9, 12, 13, 14, 16, 17, 20 and 21).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U. S. C 112

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims **1, 8 and 16** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are:

a) Claims 1, 8 and 16 recite " the delay circuit operated to delay a signal received at the control input for a predetermined amount of time and prevent a high voltage from propagating to the output if the delay circuit detects a low voltage on the signal after the predetermined amount of time". The omitted structural cooperation relationships are" the relationship or the conversion between or from "a high voltage and the low voltage" a state in the decoder" and " a soft-input value encoded with a trellis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims **1-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright et al. (U.S. PN: 6,819539).

As per claims 1, 8 and 16:

Wright et al. teach or disclosed a method for circuit recovery from overstress conditions, comprising the steps of (A) is detecting an event and (B) resetting a device when the event is a first predetermined type and providing recovery when the event is

a second predetermined type (see col. 1, lines 50-55). Further, Wright et al. in figure 5 teach a circuit (or system) 500 illustrating detection of a noise-coupling event is shown. A stress event, such as ESD, may cause circuit malfunction by coupling noise onto a critical node, with or without an over/under-voltage. The circuit (500) generally, comprises a pad (502), a pad (504), an oscillator circuit (506) (to generate a signal and to present to a tunable delay circuit (508), (the delay circuit configured to present a signal to a short pulse detect circuit (510) (see col. 5, lines 16-30). Wright et al. **do not explicitly** teach the delay circuit delays a signal and prevent high voltage from propagating to the output of the delay circuit if the delay circuit detects a low voltage. **However,** Wright et al. in figure 4 teach that a circuit (or system) 400 for detecting under-voltages comprises a pad circuit 402, a pad 404 a resistance block 406, a transistor 408, a resistance block 410 and a register 412 whereby the register 412 may be configured to generate (and/or store) a signal (e.g. EVENT_UNDER). The signal EVENT_UNDER may be configured as a fault causing event signal and the signal EVENT_UNDER may be configured as an under-voltage event signal. The circuit 400 may operate similarly to the circuit 300 (in figure 3) where the NMOS device 400 may remain off, until an under-voltage event sufficiently below ground voltage causes current flow, setting the output EVENT_UNDER which Wright is basically teaching the same system as the applicant's invention to detect and delay high voltages or over-voltages. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to detect and delay on the output or input signals as taught by Wright et al. This modification would have been obvious because

a person having ordinary skill in the art would have been motivated to do so because providing a detecting and delaying circuits are well known features of ESD event circuit.

As per claim 2:

Wright et al. teach all the subject matter claimed in claim 1 including Wright et al. teach an oscillator circuit (506) (to generate a signal and to present to a tunable delay circuit (508), (the delay circuit configured to present a signal to a short pulse detect circuit (510) (see col. 5, lines 16-30).

As per claim 3:

Wright et al. teach all the subject matter claimed in claim 1 including Wright et al. in figures 1a and 1b a process (or method) (100) may allow recovery from circuit stress conditions (or events) that may cause a device to stop operating properly. In particular, the process 100 may apply to microcontrollers and systems that execute firmware to provide recovery from overstress conditions (to be described in connection with FIG. 2). Stress conditions include those covered by industry standard tests for electrostatic discharge (ESD), electrical fast transient/burst (EFTB), radiated EMI, and operation in severe environments where significant noise coupling may occur and upset the operation of an electronic device (see col. 2, lines 26-48).

As per claim 4:

Wright et al. teach all the subject matter claimed in claim 1 including Wright et al. teach an oscillator circuit (506) (to generate a signal and to present to a tunable delay

circuit (508), (the delay circuit configured to present a signal to a short pulse detect circuit (510) (see col. 5, lines 16-30).

As per claims 5-7:

Wright et al. teach all the subject matter claimed in claim 1 including Wright et al. teach a resistance block (RLOAD) 310 may be implemented as an inductor configured to generate a voltage pulse in response to a current pulse. The resistance block (RLOAD) 310 may then provide a pulse to trigger the event detect register 312 (see col. 4, lines 7-29).

As per claim 9:

Wright et al. teach all the subject matter claimed in claim 8 including Wright et al. teach an oscillator circuit (506) (to generate a signal and to present to a tunable delay circuit (508), (the delay circuit configured to present a signal to a short pulse detect circuit (510) (see col. 5, lines 16-30).

As per claims 10 and 11:

Wright et al. teach all the subject matter claimed in claim 8 including Wright et al. in figures 1a and 1b a process (or method) (100) may allow recovery from circuit stress conditions (or events) that may cause a device to stop operating properly. In particular, the process 100 may apply to microcontrollers and systems that execute firmware to provide recovery from overstress conditions (to be described in connection with FIG. 2). Stress conditions include those covered by industry standard tests for electrostatic discharge (ESD), electrical fast transient/burst (EFTB), radiated EMI, and operation in

severe environments where significant noise coupling may occur and upset the operation of an electronic device (see col. 2, lines 26-48).

As per claims 12-15:

Wright et al. teach all the subject matter claimed in claim 8 including Wright et al. teach a resistance block (RLOAD) 310 may be implemented as an inductor configured to generate a voltage pulse in response to a current pulse. The resistance block (RLOAD) (310) may then provide a pulse to trigger the event detect register 312 (see col. 4, lines 7-29).

As per claim 17:

Wright et al. teach all the subject matter claimed in claim 16 including Wright et al. teach an oscillator circuit (506) (to generate a signal and to present to a tunable delay circuit (508), (the delay circuit configured to present a signal to a short pulse detect circuit (510) (see col. 5, lines 16-30).

As per claims 18 and 19:

Wright et al. teach all the subject matter claimed in claim 8 including Wright et al. in figures 1a and 1b a process (or method) (100) may allow recovery from circuit stress conditions (or events) that may cause a device to stop operating properly. In particular, the process 100 may apply to microcontrollers and systems that execute firmware to provide recovery from overstress conditions (to be described in connection with FIG. 2). Stress conditions include those covered by industry standard tests for electrostatic discharge (ESD), electrical fast transient/burst (EFTB), radiated EMI, and operation in

severe environments where significant noise coupling may occur and upset the operation of an electronic device (see col. 2, lines 26-48).

As per claims 20-21:

Wright et al. teach all the subject matter claimed in claim 8 including Wright et al. teach a resistance block (RLOAD) 310 may be implemented as an inductor configured to generate a voltage pulse in response to a current pulse. The resistance block (RLOAD) 310 may then provide a pulse to trigger the event detect register (312) (see col. 4, lines 7-29).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,744,291 Payne et al.

US PN: 6,765,771 Ker et al.

US PN: 6,862,161 Woo

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Art unit: 2133

GUY LAMARRE
PRIMARY EXAMINER